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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TUCKER, WESLEY J	

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,785	ROYLANCE, EUGENE A.	
	Examiner	Art Unit	
	Wes Tucker	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,9-14 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9-14 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 9th 2005 has been entered.

Response to Amendment and Arguments

1. Applicant's response to the last office action, filed May 9th 2005, has been entered and made of record.

2. Applicant has cancelled claims 2, 7, 8 and 15. Applicant has amended claims 1, 16 and 20. Claims 1, 3-6, 9-14 and 16-25 are pending.

3. Applicant's arguments have been fully considered and entered, but are not completely persuasive for at least the following reasons:

4. Applicant has amended the independent claims 1, 16 and 20 to include the new limitation that each bus interface is "selectively programmably configurable" and controllable with programming control input. Applicant also argues that the combination of references to Lee and Kiuchi does not teach the

elements claimed in independent claims 1, 16 and 20. The following limitations are addressed:

1. Applicant argues that Lee and Kiuchi do not disclose having multiple support buses, rather they employ a single high bandwidth bus that is always coupled to each of the image processing modules. Examiner points to the fact that Lee discloses a memory bus, (Fig. 1, element 14, referred to as an image ring bus) as well as a first support bus (Fig.1, element 50, referred to as the system bus). Lee does not disclose multiple support buses, however the motivation to include one support bus or a second bus is the same as any additional support buses. Kiuchi teaches that six support buses are used to execute digital signal processing more efficiently by enabling parallel processing and communication (column 42, lines 51-57). Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use more than one support bus to enable such efficient parallel processing and therefore it is considered justified to combine the references of Lee and Kiuchi.

2. Applicant argues that Lee and Kiuch do not teach having a separate bus interface for each image processing module or any other capability that allows for selective operative coupling of individual modules to different support buses. Examiner points to the passage in Lee (column 3, line 66-column 4, line 5). Each processing unit 58A-58D contains an interface to the local buses 68A-68D. The interfaces which couple the processing units 58A-58D to the local buses also couples the processors to the image ring bus 53 though the modules

60A-60D through 64A-64D. Therefore the same logic mentioned above in the combination of Kiuchi and Lee of using more than one support bus also applies to the coupling through interfaces.

3. Applicant argues that Lee and Kiuchi do not disclose having at least two logic modules configured to selectively process image related data according to different image processing algorithms, but rather the logic modules have different fields of view, and wherein the control signal causes selective routing of image data between logic modules though an operatively coupled support in accordance with a data processing order. Examiner points to the passage in Lee (column 4, line 60–column 5, line 5) wherein an architecture example of the invention is shown and wherein the different processors are configured so that each processor has its processing elements specialized for different image processing functions. This is considered to read on different image processing algorithms.

4. Applicant argues that Lee and Kiuchi do not disclose bus interfaces that are selectively programmably configurable to operatively couple logic modules to at least a programmably selected one of the first support bus and the second support bus in response to at least one programming control input to selectively route at least a portion of the image related data between the at least two logic modules for processing in accordance with a programmable data processing order. Examiner points to the passage in Lee (column 3, lines 35-45) wherein it is disclosed that the host computer 36 controls the operation of each of

the image processing modules as well as the disk image interface 16 to the buses. Therefore the host computer would also be responsible for coupling the processors to either the image ring bus or the system bus by controlling the interfaces which would inherently involve programmably selecting where image data would be transferred and on which bus. Further in the passage (column 3, line 66-column 4, line 5) it is disclosed that the ASIC controller interfaces to the local buses and that there are any number of floating point controllers in the architecture. Therefore the bus interfaces must be programmably configurable.

Therefore the rejection in view of Lee and Kiuchi is maintained and the discussion of claim 1 above, also applies to claims 16 and 20.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, and 9-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patent 6,130,967 to Lee et al. and U.S. Patent 6,304,958 to Kiuchi et al.

2. With regard to claim 1, Lee discloses an apparatus comprising a plurality of logic modules, wherein at least two logic module being configured to

selectively process image related data according to a different image processing algorithm (Fig.3A, elements 170-174, column 4, lines 60-62).

A plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module (Fig.1, elements 24, and 16, and Fig. 2, elements 70, 58A-58D and column 3, lines 55-58);

A plurality of buses including at least a memory bus, and a first support bus, wherein each bus interface is selectively programmably configurable to operatively couple the corresponding logic module to at least a progammably selected one of the first support bus in response to at least one control input to selectively route at least a portion of the image related data between at least two logic modules for processing in accordance with a programmable data processing order (Fig.2, elements 56 and 70, column 3, lines 55-68). Here Lee discloses an interface to pass image data to the logic modules (56) and an interface to connect to the logic modules from the system bus (70).

Lee discloses that each of the plurality of field of view modules (Fig.1, elements 24-34) are coupled to the system bus (Figs.1 and 2, element 50) by interfaces (Fig. 2, element 70) and that each processing unit contains multiple buses (68A-68B), each of which also has a processing unit or interface (58A-58D) for its respective bus. Lee also discloses an image bus ring (Fig.1, element 14 and column 3, lines 36-42) that enables fast communication between image processing modules. The image bus ring is also connected to interfaces (16 and 24).

Lee discloses the memory bus and the first support bus, but does not disclose the use of an additional second support bus. Kiuchi discloses a microcomputer configuration (Fig. 34) for use in performing digital signal processing with multiple support buses as well as multiple memory address buses and multiple execution units or logic modules. Kiuchi teaches that the six support buses are used to execute the digital signal processing more efficiently (column 42, lines 51-57). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use multiple support buses in order to increase the efficiency of digital signal processing as taught by Kiuchi in the digital image processor of Lee.

4. With regard to claim 3, Lee discloses the apparatus as recited in Claim 1, further comprising a memory bus interface (Fig. 1, elements 16 and 20) operatively coupled to the memory bus (Fig. 1, element 14 or 50). Here the memory bus can be considered to be either the image bus ring (14) or the system bus (50) both of which are coupled to the image discs array (18), which is interpreted as a memory where image information is stored. The buses are coupled through the interfaces (16 and 20).

5. With regard to claim 4, Lee discloses the apparatus as recited in Claim 3, wherein the memory bus interface (Fig.1, element 16) is further configured as a memory controller and configurable for use with memory. Here

Lee discloses a memory bus interface (16), which is coupled to a computer system interface (20), which is attached to the memory (18) or image disc array. The combination of the interfaces, (16 and 20) are configured together as a memory controller/interface.

6. With regard to claim 5, Lee discloses the apparatus as recited in Claim 4, further comprising memory (Fig.1, element 18) operatively coupled to the memory bus interface (Fig.1, elements 16 and 20). Here Lee discloses that the memory or image discs array (18) is coupled to the memory bus (14 or 50) through interfaces (16 and 20).

7. With regard to claim 6, Lee discloses the apparatus as recited in Claim 5, wherein the memory bus (50) is configured to selectively route the image related data between the memory (18) and at least one of the plurality of logic modules (28-34) via the bus interface (Fig. 2, element 70) associated with the at least one logic module and the memory bus interface. The system bus (50) is interfaced with the memory (18) through interfaces (16 and 20) and the image data is routed to the logic modules (28-34) through separate interfaces (Fig.2, element 70). Fig.2 is a diagram of one of the plurality of logic modules interfaced.

10. With regard to claim 9, Lee discloses the apparatus as recited in Claim 8, wherein at least two of the plurality of logic modules are configured to share information by sending and receiving one or more messages via at least one of the plurality of buses (column 3, lines 40-42). It is understood that the messages read on the control data for identifying the transmissions of data.

11. With regard to claim 10, Lee discloses the apparatus as recited in Claim 9, wherein the message includes at least one identifier selected from a group of identifiers comprising a destination identifier (column 4, lines 58-62). To send and receive information there is an identifier for where the information is going and where the information is coming from is specified. A destination identifier must be named for the image data in order for the correct processor to perform its respective function.

12. With regard to claim 11, Lee discloses the apparatus as recited in Claim 9, wherein the message includes a data field capable of carrying the image related data (column 4, lines 58-62). It is understood that the image data must be accompanied by attribute data in order to route the image to the correct processor with the correct respective algorithm.

13. With regard to claim 12, it is understood that the image data field of the message contains image data or information related to image data. The

image data must be accompanied by attribute data for the same reasons discussed in claims 11 and 12.

14. With regard to claim 13, Lee discloses the plurality of image processing modules perform a filtering operation (column 2, lines 5-15).

15. With regard to claim 14, Lee discloses that the data processing order is associated with an image-processing pipeline (column 4, lines 60-68).

16. With regard to claim 15, Lee discloses that for each bus interface the data processing order is established via the control inputs (column 4, lines 55-60). Lee discloses that the processors can be configured to perform different image processing. Fig.3A displays a routing unit that determines which processors the image data is sent to in order to perform image-processing functions.

17. With regard to claim 16, Lee discloses an apparatus comprising: a plurality of logic modules (Fig.1, elements 28-34 and Fig.2, elements 170-174), each logic module being configured to selectively process image related data according to a different image processing algorithm (column 4, lines 60-65).

Lee further discloses a plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module (Fig.2, elements 70 and 56).

Fig.2 is a representation of each of the processing modules and each module is coupled to two different buses via two different interfaces (56 and 70).

Lee further discloses a plurality of buses, including al least a memory bus, and a first support bus (Fig. 1, elements 14 and 50), operatively coupled to the plurality of bus interfaces (Fig.2, elements 56 and 70), and wherein each of the plurality of bus interfaces is selectively programmably configurable to selectively route image related data through the first support bus to the corresponding logic modules for processing in accordance with a programmable data processing order (Fig.1, element 50 and Fig. 2, elements 56 and 70).

Lee discloses that each of the plurality of field of view modules (Fig.1, elements 28-34) are coupled to the system bus and image ring bus (Figs.1 and 2, elements 50 and 14) by interfaces (Fig. 2, elements 70 and 56) and that each processing unit contains multiple buses (68A-68B), each of which also has a processing unit or interface (58A-58D) for its respective bus. Lee also discloses an image bus ring (Fig.1, element 14 and column 3, lines 36-42) that enables fast communication between image processing modules. The image bus ring is also connected to interfaces (16 and 24).

Lee discloses the memory bus and the first support bus, but does not disclose the use of an additional second support bus. Kiuchi discloses a microcomputer configuration (Fig. 34) for use in performing digital signal processing with multiple support buses as well as multiple memory address buses and multiple execution units or logic modules. Kiuchi teaches that the six

support buses are used to execute the digital signal processing more efficiently (column 42, lines 51-57). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use multiple support buses in order to increase the efficiency of digital signal processing as taught by Kiuchi in the digital image processor of Lee.

18. With regard to claim 17, Lee discloses the apparatus as recited in Claim 16, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data (column 3, lines 35-42). Lee references pixels being transferred as a type of image data, it is understood that pixel data must be transferred along with address data such as pixel position in the image and index data such as what image the pixels belong to. These kinds of descriptive data are inherent to the function of transferring image data

19. With regard to claim 18, Lee discloses a filtering operation on the image data (column 2, lines 10-15).

20. With regard to claim 19, Lee discloses the apparatus as recited in Claim 17, wherein the programmable data processing order causes an image processing pipeline to be formed using at least a portion of the plurality of logic modules (column 4, lines 55-68).

21. With regard to claim 20, Lee discloses an image processing device comprising:

a plurality of buses, including at least a memory bus (Fig.1, element 14), and a first support bus (Fig.1, element 50);

memory suitable for storing image related data (Fig.1, element 18);

a memory bus interface (Fig.1, elements 16 and 20) coupled to the memory bus (Fig.1, element 14 or 50) and the memory and configured to provide access to the memory via the memory bus. Lee discloses the image ring bus (14) enabling high-speed access between the image disc array or memory (18) and the image processors (28-34).

Lee further discloses a plurality of logic modules (Fig.1, elements 28-34), each logic module being configured to process image related data according to process image related data according to a different image processing algorithm (column4, lines 60-65).

Lee further discloses a plurality of bus interfaces (Fig.2, elements 56 and 70), each bus interface being coupled to a corresponding logic module (Fig.1, elements 28-34), the first support bus, and the memory bus (Fig.1, elements 50 and 14), and configurable to selectively route the image related data through the first support bus and the memory bus to the plurality of logic modules for processing in accordance with a data processing order (column 3, lines 30-42).

Lee discloses the memory bus and the first support bus, but does not disclose the use of an additional second support bus. Kiuchi discloses a microcomputer configuration (Fig. 34) for use in performing digital signal processing with multiple support buses as well as multiple memory address buses and multiple execution units or logic modules. Kiuchi teaches that the six support buses are used to execute the digital signal processing more efficiently (column 42, lines 51-57). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use multiple support buses in order to increase the efficiency of digital signal processing as taught by Kiuchi in the digital image processor of Lee.

22. With regard to claim 21, Lee discloses the image processing device of claim 20, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data (column 3, lines 35-42 and column 4, lines 55-65). Lee discloses an image bus ring enabling communication between the plurality of logic units and processors in order to perform different operations on the image data at each processor or logic unit. Therefore destination or address data and image data must both be transmitted to enable the transfer of image data to the correct processing unit.

23. With regard to claim 22, Lee discloses the plurality of image processing modules perform a filtering operation (column 2, lines 5-15).

24. With regard to claim 23, Lee discloses a pipeline using the plurality of logic modules (column 4, lines 55-68). Here in regard to figure 3, processors 170-174 are equivalent to the modules of figure 1, elements 28-34.

25. With regard to claim 24, Lee discloses the apparatus as recited in claim 20, wherein the data processing order is established via control inputs to the plurality of bus interfaces (Fig.2, elements 56 and 70 and Fig.1, elements 28-34). To transfer to the multiple processing units it is inherent that processing order be determined by control received at the bus interfaces.

26. With regard to claim 25, Lee discloses the method and apparatus to be used with an image inspection device (column 1, lines 55-60). It is understood that the image-processing device may be used in any image-processing environment that is found to be beneficial.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wes Tucker whose

telephone number is 703-305-6700. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on (703) 308-6604. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wes Tucker

7-7-05

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PRIMARY EXAMINER